15.1 A 390Mb/s 3.57mm² 3GPP-LTE Turbo Decoder ASIC in 0.13µm CMOS

Christoph Studer, Christian Benkeser, Sandro Belfanti, Quting Huang

1ETH Zürich, Zürich, Switzerland
2Advanced Circuit Pursuit, Zollikon, Switzerland

Recent popularity of smart phones, netbooks, and other mobile broadband devices has vindicated 3G (WCDMA/HSPA) as an enabling technology for main-stream high-speed data and has given fresh impetus to its 4G successor, LTE (Long-Term Evolution). With mass deployment anticipated in 2-to-3 years, development of cost-effective and low-power LTE user equipment is currently keeping the wireless industry preoccupied. While the 1st-generation terminals will target 100Mb/s in the downlink, the MIMO-based LTE standard is capable of 326.4Mb/s [1] operation, which is more than 20× that of HSDPA. As with HSDPA, turbo decoding will be among the challenges (along with MIMO detection) in computation intensity, now threatening to be 20× higher. This contributes to the feasibility of achieving the LTE maximum throughput with a turbo decoder ASIC realization, and the 100Mb/s milestone with competitive power consumption and die area.

Our previous work [2] discusses a variety of techniques applied to a turbo decoder to achieve 10.8Mb/s, and especially focuses on: (1) the add-compare-select (ACS) circuit extensively used in the maximum a-posteriori (MAP) decoder, as well as (2) the interleaved address generation. Address conflicts inherent to HSDPA, however, preempt any parallel processing.

LTE specifies contention-free interleaving, which enables both the trellis and the memory storing its corresponding log-likelihood ratios (LLRs) in natural order to be divided into (up to) 8 equal segments, even for the smallest block size. For every octet of equidistant steps from the 8 trellis segments, the corresponding LLRs in either natural or interleaved order are located at equidistant addresses in the 8 memory segments (shown in Fig. 15.1.1). By folding the memory appropriately, up to 8 trellis segments can be processed by separate MAP decoders concurrently without conflict in memory access. Figure 15.1.1 also shows how throughput can be improved by such parallelism and the use of radix-4 computations without resulting in a dramatic increase in silicon area, and where the critical path and hence the maximum clock rate, is not affected by the parallelism.

Radix-4 computation is realizable at moderate complexity because the LTE interleaver maps odd addresses to other odd addresses and even to even, so that 2 trellis steps can be computed per clock cycle [3]. Clearly both radix-4 computations and parallel MAP decoders are necessary for the maximum LTE throughput for 0.13µm CMOS, even though parallel and interleaved access to memories at the double speed of radix-4 (compared to radix-2) is non-trivial.

The general tradeoffs shown by Fig. 15.1.1 remain valid for other technology nodes.

Figure 15.1.2 shows the architectural diagram of our turbo decoder ASIC, where memory access receives particular attention. It consists of 8 parallel radix-4 MAP decoders, input memories for systematic LLRs, parity-(1,2) LLRs, intermediate memories to store (between turbo half-iterations) computed a-posteriori extrinsic LLRs, a 3GPP-LTE address generator, and Batch networks [4] in master/slave configuration for assigning interleaved memory contents to the parallel decoders.

The input and intermediate memories store up to 6144 LLRs (in support of the maximum LTE codeword block size), to which 8×2 accesses for systematic, extrinsic, and parity LLRs are required per clock cycle. To permit interleaved access during half-iterations, the systematic and intermediate RAMs are both split into 2 instances, each holding 8 LLRs per row for either odd or even trellis steps; this configuration enables 3×8×2 LLR-values to be read per clock cycle.

Figure 15.1.3 presents our approach to the parallel storage and distribution of 3×8×2 LLRs for 8 MAP decoders in natural and interleaved order, which is generally applicable to contention-free interleaving. In each clock cycle all required (LLR) addresses for the odd and even octets of trellis steps (corresponding MAP decoders) must be computed. The address generator does this recursively, taking advantage of the recursive formulation of consecutive addresses by the quadratic permutation polynomial (QPP) interleaver used in LTE, and only requires additions and ACS-based module computations.

There are several ASIP configurations without resulting in a dramatic increase in silicon area. This contributes to the feasibility of achieving the LTE maximum throughput with a turbo decoder ASIC realization, even though parallel and interleaved access to memories at the double speed of radix-4 (compared to radix-2) is non-trivial.

The critical path in the radix-4 ACS units is optimized for decoder throughput. Module normalization [2] simplifies the implementation and the selection is carried out by 6 parallel comparators followed by a look-up table, which shortens the critical path by 50% (from a tree-like radix-4 ACS implementation) at negligible area overhead.

The hardware-friendly max-log approximation in the MAP decoders causes a mismatch in the output LLRs. To solve this, the LSQs with a constant factor of 0.6875 (Fig. 15.1.2) partially compensates this mismatch at negligible overhead [2]. Figure 15.1.5 shows that minimizing scaling improves the BER performance of the turbo decoder by more than 0.2dB. Compared to an ideal turbo decoding algorithm (floating-point using the sum-product algorithm), our implementation only requires 0.14dB higher SNR for the same BER.

Figure 15.1.6 summarizes the key characteristics of the turbo decoder ASIC and provides comparison with published turbo decoder implementations [6,5,2,3] for LTE and HSDPA, including normalized hardware efficiency (in MB/s/mm²). The 3.57mm² chip in 0.13µm CMOS comprises 55k gates and 129kb of RAM. The maximum clock frequency is 302MHz, at which a throughput of 390.6Mb/s on 5.5 iterations is measured. The theoretical LTE maximum can therefore be achieved with margin. At the more realistic 100Mb/s throughput targeted by industry today, the measured power consumption is 68.6mW, and the corresponding energy efficiency is 0.13nJ/bit/iteration. In addition to outstanding turbo-decoding throughput, both ultra low-power and cost-effectiveness are demonstrated by the present ASIC prototype.

Acknowledgments:

The authors would like to thank S. Schläfer, F. Gürkaynak, N. Felber, and W. Fichtner for their support during the ASIC design.

References:

Figure 15.1.1: Top: contention-free interleaver; bottom: radix-2 and radix-4 turbo-decoder tradeoffs (for maximum clock rate in 0.13µm CMOS).

Figure 15.1.2: Architectural diagram of the turbo decoder.

Figure 15.1.3: LTE interleaver architecture.

Figure 15.1.4: Radix-4 max-log-MAP decoder with modulo-normalization.

Figure 15.1.5: BER performance over an AWGN channel (block size 3200).

Figure 15.1.6: Comparison of key characteristics to other turbo decoders.